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10/070,256	03/04/2002	Norihiko Sugita	TAMA 0002	2968

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/070,256	SUGITA ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites unclear limitations of "said mounting pad is separated into an area ...at relatively low speed" implying that one mounting pad is divided into regions which can conduct different several signals. However, the instant invention discloses through the Figures that a mounting pad is a conducting point for a specific signal and the device mounting area is divided into different regions operating at a specific signal speed.

Claim 1 further recites "the external connecting electrodes corresponding to an address output and a data input-output are arranged on *a rear face of said area* for mounting the plural semiconductor integrated circuit chips..." does not convey a clear meaning. In addition, it is not clear which chip is connected to the address output and the data input/output.

Claims 4 and 8 recite the similar limitation in an identical manner recited in claim 1 above.

Claim 2 recites "many external connecting electrodes allocated to the supply of a power voltage and a ground voltage are arranged on a rear face of said area for mounting the plural semiconductor integrated circuit chips operated at relatively high speed." However, Fig. 2 of the

Application shows that external connecting electrodes for power and grounds are distributed all over the mounting space including the regions for a high and a low speed device.

Claims 5 and 10 recite the similar limitation in an identical manner recited in claim 2 above.

Claim 3 recites "said wiring layers on the other face of said module substrate." However, Figures of the Application show that the wiring layers built in the module substrate.

Claims 6 recites "wherein the external connecting electrodes for operating power allocated to supply a power voltage and a ground voltage are coarsely and closely arranged on the module substrate, and are closely arranged on rear faces of the semiconductor integrated ...." The limitation of "coarsely and closely arranged" conveys a contradictive meaning.

Claim 7 recites a limitation "...said mounting pattern includes a grouped pattern able to arrange semiconductor integrated circuit chips approximately having an equal height size in one line and mount these semiconductor integrated circuit chips every group of the semiconductor integrated circuit chips; and the mounting pattern and a bump electrode of the semiconductor integrated circuit chip are electroconductively connected to each other through an anisotropic electroconductive film stuck every said grouped pattern" which conveys a unclear meaning. Examiner assumes this limitation implying that chips of the same kind are arranged in a group.

Claim 8 recites a limitation of "an electronic circuit including a first semiconductor device and a second semiconductor device able to be operated at high speed in comparison with said first semiconductor device wherein the first and second semiconductor devices are mounted to a bus of a wiring substrate in a common connecting state" indicating that the first device operates at a lower speed, thus the first device is a buffer device as disclosed in the Applicant's

specification . However, claim 8 further recites a limitation of "said second semiconductor device has a data processor chip and a memory chip commonly connected to said bus through an external connecting electrode in a multilayer wiring substrate, and includes a buffer circuit" indicating that this buffer circuit (device) operates at higher speed. Consequently, claim 8 recites the limitations indicating that a buffer circuit operates at high and low speed. And this aspect is not disclosed in the specification.

Claims 9 and 10 recite a limitation of "said buffer circuit is ...into said wiring path." Note that a buffer circuit requires other signal lines in addition to the ones recited in the claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oyama (JP 10-12809) in view of Yoshikawa (US 6199150).

Regarding claim 1, insofar as understood, Fig. 1(a) of Oyama shows a multichip module including a module substrate (1) having plural wiring layers (10, 11), many external connecting electrodes (3, 4, 5) formed on one face of said module substrate and a mounting region for mounting plural semiconductor integrated circuit chips (21, 22) formed on the other face of said module substrate;

wherein the mounting region is separated into an area of the mounting the plural semiconductor integrated circuit chips as shown in Fig. 1(b) for input/out signals (3) and a power/ground voltage (4).

Note that mounting pads are needed to mount the chips on a wiring substrate (a module substrate).

Oyama shows the most aspect of the instant invention except that a mounting region is separated into an area of the mounting pad of the plural semiconductor integrated circuit chips able to be relatively operated at high speed, and an area of the mounting pad of the plural semiconductor integrated circuit chips operated at relatively low speed and the external connecting electrodes corresponding to an address output and a data input-output are arranged on the other face of said area for mounting the plural semiconductor integrated circuit chips operated at relatively low speed.

Fig. 1 of Yoshikawa shows a device mounting area is divided into regions for a high speed device and a low speed device and an address can be output to a low-speed device (col. 5, lines 7-13) while a data can be accessed and stored at low speed (col. 2, lines 27-33). Note that an external connecting electrodes is needed to connect these address and date line to the mounting board.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Yoshikawa into the device of Oyama in order to arrange the chips in high speeding and low speeding areas to improve the efficiency of the memory system.

Claims 3, 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oyama in view of Smits et al. (US 5432913), hereafter Smits.

Regarding claim 3, insofar as understood, Fig. 1(a) of Oyama shows a multichip module including a module substrate (1) having plural wiring layers (10, 11), many external connecting electrodes (3, 4, 5) formed on one face of said module substrate and plural semiconductor integrated circuit chips (21, 22) formed the other face of said module substrate.

Oyama fails to show that plural semiconductor integrated circuit chips are processor chip, memory chips and buffer circuits and "wherein the data processor chip is arranged approximately at the center of said module substrate, and the plural memory chips are arranged on one side and the plural buffer circuits are arranged on the other side in parallel with each other through said data processor chip." Fig. 4A of Smits shows a module wherein the data processor chip (CPU) is arranged approximately at the center of the module, and the plural memory chips (SRAM) are arranged on one side and the plural buffer circuits are arranged on the other side in parallel with each other through said data processor chip.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Smits into the device of Oyama in order to have the recited arrangement of the chips to increase the efficiency of the date transfer.

Regarding claim 4, insofar as understood, Fig. 1(a) of Oyama shows a multichip module including a module substrate (1) having plural wiring layers (10, 11), many external connecting electrodes (3, 4, 5) formed on one face of said module substrate and plural semiconductor integrated circuit chips (21, 22) formed the other face of said module substrate.

Oyama fails to show that plural semiconductor integrated circuit chips are processor chip, memory chips and buffer circuits and "the external connecting electrodes allocated for an address and data are arranged on the rear face of an area for mounting said buffer circuit."

Fig. 4A of Smits shows a module wherein the data processor chip (CPU) is arranged approximately at the center of the module, and the plural memory chips (SRAM) are arranged on one side and the plural buffer circuits are arranged on the other side in parallel with each other through said data processor chip.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Smits into the device of Oyama in order to have the recited arrangement of the chips to increase the efficiency of the date transfer.

In addition, it would be obvious for the external connecting electrodes for an address and data (for buffers in Fig. 4A of Smits' device) are arranged on the rear face (a mounting surface) of an area for mounting said buffer circuit.

Regarding claim 7, insofar as understood, Fig. 1(a) of Oyama shows a multichip module including a module substrate (1) having plural wiring layers (10, 11), many external connecting electrodes (3, 4, 5) formed on one face of said module substrate and plural semiconductor integrated circuit chips (21, 22) formed the other face of said module substrate.

Fig. 1 of Smits shows a module comprising a CPU, memories and buffers while same kind of the devices are arranged in a region of the mounting area. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Smits into the device of Oyama in order to have the same kind of the device grouped in one region of the mounting area for compact packaging.

Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oyama in view of Sato (US 5729764).

Regarding claim 8, insofar as understood, Fig. 1(a) of Oyama shows a multichip module including a module substrate (1) having plural wiring layers (10, 11), many external connecting electrodes (3, 4, 5) formed on one face of said module substrate and plural semiconductor integrated circuit chips (21, 22) formed the other face of said module substrate.

Oyama fails to show two semiconductor devices operating at different speeds and a functionality of the buffer circuit. Fig. 1 of Sato shows an integrated circuit device comprising a CPU, a memory circuit and a buffer circuit and the buffer circuit controls(interrupts) input data through a CPU (col. 2, lines 36-64). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Sato into the device of Oyama in order to form a circuit recited in the instant invention for a desired circuit configuration. Note that it would be obvious for the memory chip and the CPU operate at higher speed than the buffer circuit since the buffer circuit disables the data outputting (col. 2, lines 53-64).
And as discussed above, it is obvious to have the external connection electrodes for an address and data for the buffer circuit arranged on the rear mounting surface of the buffer device.

Claims 9 and 10, insofar as understood, Fig. 3 of Sato shows an address input/output buffer, a control signal output buffer and a data input/output buffer respectively inserted into said wiring path; and said data input/output buffer. And Sato discloses that the buffer circuit is in a high impedance state during the data is accessed (col. 2, lines 1-5).

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oyama in view of Smits and Takemae et al. (US 6078514), hereafter Takemae.

Regarding claims 5 and 6, insofar as understood, Fig. 1(a) of Oyama shows a multichip module including a module substrate (1) having plural wiring layers (10, 11), many external connecting electrodes (3, 4, 5) formed on one face of said module substrate and plural semiconductor integrated circuit chips (21, 22) formed the other face of said module substrate.

Oyama fails to show that plural semiconductor integrated circuit chips are processor chip, memory chips and buffer circuits and wherein external connecting electrodes allocated to supply a power voltage and a ground voltage are arranged on the rear face of an area for mounting said memory chip for larger power consumption.

Fig. 4A of Smits shows a module wherein the data processor chip (CPU), the plural memory chips (SRAM) and the plural buffer circuits are arranged. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Smits into the device of Oyama in order to have the recited arrangement of the chips to increase the efficiency of the date transfer.

The combined teachings of Oyama and Smits shows the most aspect of the instant invention except "relatively many external connecting electrodes allocated to supply a power voltage and a ground voltage are arranged on the rear face of an area for mounting said memory chip." Fig. 5 of Takemae shows power supply pads (23) for power and ground in the high speed circuits (21; having lager power consumption). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Takemae into the device

of Oyama and Smits in order to arrange the external connecting electrodes (connected to the corresponding pads) for the power supply to improve the data transfer speed.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oyama and Yoshikawa as applied to claim 1 above, and further in view of Takemae.

Regarding claim 2, insofar as understood, the combined teachings of Oyama and Yoshikawa show the most aspect of the instant invention except "relatively many external connecting electrodes allocated to the supply of a power voltage and a ground voltage are arranged on a rear face of said area for mounting the plural semiconductor integrated circuit chips operated at relatively high speed." Fig. 5 of Takemae shows power supply pads (23) for power and ground in the high speed circuits (21). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Takemae into the device of Oyama and Yoshikawa in order to arrange the external connecting electrodes (connected to the corresponding pads) for the power supply to improve the data transfer speed.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oyama and Smits as applied to claim 8 above, and further in view of Takemae.

Regarding claim 11, insofar as understood, the combined teachings of Oyama and Smits show the most aspect of the instant invention except "relatively many external connecting electrodes allocated to the supply of a power voltage and a ground voltage are arranged on a rear face of said area for mounting the plural semiconductor integrated circuit chips operated at relatively high speed." Fig. 5 of Takemae shows power supply pads (23) for power and ground

in the high speed circuits (21). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Takemae into the device of Oyama and Smits in order to arrange the external connecting electrodes (connected to the corresponding pads) for the power supply to improve the data transfer speed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

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